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capacity of the memory 4 is defined as the capacity equivalent to one super frame.

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(54) DEINTERLEAVING CIRCUIT

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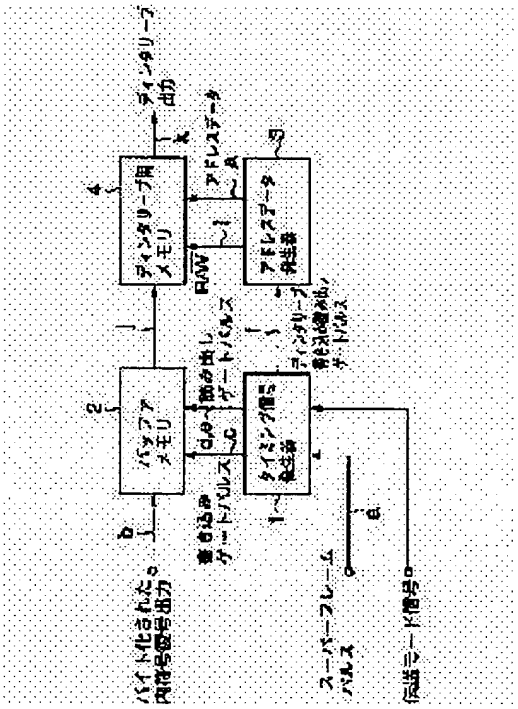

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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the day interleave circuit used for a BS-digital-broadcasting receiver.
[0002]
[Description of the Prior Art] 8x203 bytes of block interleave is performed per cutting tool, and the interleave is performed between slots with the same slot number of each frame in the direction of a super frame as the interleave method in a BS-digital-broadcasting receiver is already learned.
[0003] Here, the MPEG 2-TS packet of the main signal of a BS-digital-broadcasting signal consists of one slot formed by 1 byte of transmission multiplex control (TMCC (Transmission andMultiplexing Cofiguration Control)) signal 204 bytes, in order to show 203 bytes, a synchronizing signal, a modulation technique, error correcting system containing 16 bytes of parity for outside digital-error correction, etc., it constitutes one frame from 48 slots, and is using eight frames as 1 super frame.
[0004] In order to carry out the day interleave of the data interleaved as mentioned above, the memory which has the storage capacity for 2 super frame was required. For this reason, the memory of the storage capacity which also amounts to a maximum of 155904 bytes (=203(cutting tool) x48(slot) x8 frame x2 (super frame)) is required.
[0005]
[Problem(s) to be Solved by the Invention] However, when a day interleave circuit was constituted using the memory of the memory capacity which attains to 2 super frame like before, when a day interleave circuit was integrated-circuit-ized, the gate number increased, and also there was a trouble that a chip area will become large.
[0006] This invention aims at offering the day interleave circuit where there is little memory capacity and it ends.
[0007]
[Means for Solving the Problem] The day interleave circuit concerning this invention is a day interleave circuit in a BS-digital-broadcasting receiver. Set the number of the main signals in 1 slot to m, and the depth of a day interleave is set to n. The address number of the proper assigned to the memory for a day interleave is set to y. When the address data which specify the R/W address position of data are set to A and it presupposes that a modulo b is the remainder of a-alpha b (natural number in which alpha contains 0), It is the x-th power of A=yxn at the time of (y!=nxm -1). It is referred to as modulo (nxm -1). It is the x-th power of A=yxn about the address set number x which is the count which considered as A=y and specified even the address number y repeatedly at the time of (y=nxm -1). It is referred to as x set to A= 1 in modulo (nxm -1) at the time of y= 1. And it has an address-data generating means to generate the address data A made into A= (x-th power of yxn) when the value of the x-th power of yxn is under a value of (nxm -1). The main signal memorized by the address position of the memory specified with the address data generated by the address generation means is read, and it is characterized by writing in the following main signal which an interleave is carried out to this address position, and is inputted into it.

[0008] In the day interleave circuit concerning this invention, the main signal memorized by the address position of the memory specified with the address data A generated by the address generation means is read. Since the following main signal which an interleave is carried out [the signal] to the address position which became an opening substantially by this read-out, and is inputted into it is written in, when the day interleave could be performed with the memory capacity of the memory for a day interleave, the memory capacity of the memory for a day interleave is the memory of one half of memory capacity, and ends to the memory of the memory capacity of 2 super frame needed conventionally and it integrated-circuit-izes, there will be little need area and it will end.
[0009] m ** counter which carries out counting of the number of the main signals into which an address-data generating means is inputted in the day interleave circuit concerning this invention, S ** counter which carries out counting of the carry of m ** counter, and the multiplier which carries out the multiplication of (nxm) to the enumerated data of S ** counter, When a main signal value amounts to (m-1), carry out 1 case shift in the direction of n, and counting of the main signal is carried out in the direction of a slot. the direction of a slot -- the number of the main signals -- counting -- carrying out -- counting -- the offset value to which enumerated data carry out counting of it repeatedly similarly until at least order reaches (nxm) -- counting -- a means, the output of a multiplier, and an offset value -- counting -- it has an addition means to add counting of a means, and is characterized by using the output of an addition means as address data A.
[0010] A day interleave is performed by reading the main signal from the address position of memory specified with the address data outputted from an address generation means, and being written in.
[0011]
[Embodiment of the Invention] Hereafter, the gestalt of operation of the day interleave circuit concerning this invention explains.
[0012] Drawing 1 is the block diagram showing the configuration of the day interleave circuit concerning one gestalt of operation of this invention. As for the day interleave circuit concerning one gestalt of operation of this invention, trellis sign method (trellis sign method is hereafter described as TC) 8PSK (rate r=of coding 2/3) has illustrated the case where the method type QPSK of 46 slots, convolutional-code-izing, and blowout CHADO encoding (rate r=of coding 1/2) is one slot.
[0013] Drawing 3 (a) shows the super frame pulse a outputted synchronizing with each super frame. The inner sign decode data b shown in drawing 3 (b) decoded and cutting-tool-ized by the trellis and the Viterbi decoder which are a decoder to the output by which received the BS-digital-broadcasting signal and inner sign decode was carried out (cutting tool unit), i.e., a trellis sign, and a convolutional code are outputted synchronizing with the super frame pulse a. The inner sign decode data b are written in buffer memory 2 in response to the write-in gate pulse c shown in drawing 3 (c) outputted from the timing signal generator 1 which received the super frame timing signal and the transmission-mode signal.
[0014] 203 bytes of main signal is written in the buffer memory 2 which consists of FIFO by the write-in gate pulse c, and this writing is memorized. It dissociates, and a synchronizing signal, a TMCC signal, and a burst symbol signal are not written in buffer memory 2, but non-data are written in at this period. In drawing 3 (c), 4 bytes of notation shows the burst symbol period.
[0015] Here, depending on a modulation technique and the rate of coding, the data rate of the data rate of the cutting-tool-ized data is 1/2 with 1, then a QPSK sign (rate r=of coding 1 / 2 (rate r=of coding 1/2 may omit hereafter)) about the data rate of a TC8PSK sign (rate r=of coding 2 / 3 (rate r=of coding 2/3 may omit hereafter)). Therefore, with this 1 gestalt, it is the case where 8PSK signs are 46 slots and a QPSK sign is one slot, the information bit transmission efficiency of a QPSK sign is 1/2 in the case of 8PSK signs, and since the modulation of symbol rate regularity is carried out, a transmission slot turns into two slots and turns into 48 slots at one frame.
[0016] Moreover, with a BPSK sign (rate r=of coding 1 / 2 (rate r=of coding 1/2 may omit hereafter)), a data rate is 1/4. Moreover, the synchronizing signals and the TMCC signal sections which are transmitted by BPSK (rate r=of coding 1/2) are one fourth of data rates to the data rate of TC8PSK, 4 bytes of burst symbol signal is transmitted by QPSK (rate r=of coding 1/2), and the data rates of a burst symbol signal are one half of data rates.

[0017] In response to the write-in gate pulse c outputted from the timing signal generator 1, it is as the performing [a TMCC signal and a burst symbol signal are separated from the main signal in the case of writing, and / the writing to buffer memory 2] above to the buffer memory 2 of 203 bytes of main signal.
[0018] The inner sign decode output b written in buffer memory 2 From the generating stage of the read-out start pulse d shown in drawing 3 (d) which set predetermined time difference from the super frame pulse shown in drawing 3 (a) In response to the read-out gate pulse e shown in drawing 3 (e) outputted from the timing signal generator 1, period read-out of a TMCC signal and a burst symbol signal is stopped substantially. 203 bytes of main signal j (a publication of 203 bytes of cutting tool may be omitted hereafter) is burstily read from buffer memory 2 at a fixed rate. Furthermore, the day interleave writing and the read-out gate pulse f which are shown [drawing 3 (f), (a part being expanded to drawing 3 (g) and it being shown), and] in the address-data generator 3 from the timing signal generator 1 are outputted.
[0019] The R/W signal i shown in the address data A shown in drawing 3 (h) from day interleave memory writing and the address-data generator 3 which received the read-out gate pulse f, and drawing 3 (i) is outputted to the day interleave memory 4. 203 bytes of main signal j shown in drawing 3 (j) is written in the day interleave memory 4 one by one. Based on read-out addressing, a day interleave is performed on the occasion of read-out from the day interleave memory 4, and 203 bytes of main signal k shown in drawing 3 (k) by which the day interleave was carried out is outputted from the day interleave memory 4.
[0020] The R/W signal i is read at the time of high potential, directions are performed, when it is low voltage, it writes in, directions are performed and the main signal supplied to the address with which the main signal j was read by addressing by address data A at the degree is written in.
[0021] Next, based on drawing 2 , it explains to a detail further. Drawing 2 shows the data frame configuration for every processing process in one gestalt of this operation.
[0022] Drawing 2 (a) shows the inner sign decode data b supplied to buffer memory 2. The inner sign decode data b shown in drawing 2 (a) are a TC8PSK signal about 46 slots. The frame structure for 1 super frame in the case of transmitting one slot by the QPSK signal (rate r=of coding 1/2) is shown. 12 bytes of synchronization and a TMCC signal are followed. 203 bytes of main signal of TC8PSK, 4 bytes of null section, 203 bytes of main signal equivalent to a burst symbol signal, 4 bytes of null section equivalent to a burst symbol signal, --, 203 bytes of main signal of QPSK (rate r=of coding 1/2), One frame consists of 4 bytes of the null sections equivalent to a burst symbol signal, and 1 super frame consists of eight frame [0th] - frame [7th] frames.
[0023] Only the section of high potential [gate pulse / this] is written in buffer memory 2 by the write-in gate pulse c, and the data stream of the inner sign decode data b shown in drawing 2 (a) is memorized. As shown in drawing 2 (b), the main signal, i.e., a synchronizing signal, a TMCC signal, and signals other than the burst symbol signal section are written in buffer memory 2.
[0024] In the timing signal generator 1, fixed time delay was carried out in response to the super frame pulse a, and it reads, and start signal d is generated, it reads by this timing, and a gate pulse e is outputted. In response to the read-out gate pulse e, read-out is performed at a fixed rate from buffer memory 2. Let a read-out rate be the rate of 8PSK which is a base rate.
[0025] the read-out gate pulse e -- 48 bytes of synchronization, and a TMCC signal section pause -- carrying out -- 203 bytes -- reading -- 4 bytes -- stopping -- 203 bytes -- reading -- 4 bytes -- stopping -- and 203 bytes -- stopping -- 4 bytes -- stopping -- ** -- ** It is because the data rate writes in that a synchronization and the TMCC signal section become 48 bytes, and it was 1/4, so it sometimes becomes with the 4 times (12 byte x4=48) at the time of read-out.
[0026] Although the transmission slots are two slots since it is 1/2 in the case of a TS8PSK sign and, as for having considered as the 203-byte pause at the last, the modulation of symbol rate regularity is carried out, as for the information bit transmission efficiency of the QPSK sign of the main signal, it is for becoming 203 bytes and inserting dummy data in this part by inner sign decode. Drawing 2 (c) shows signs that dummy data was inserted in the part considered as the 203-byte pause.

[0027] In addition, although a burst symbol signal is not written in buffer memory 2 here, a burst signal may also be written in with the main signal, and you may read. In this case, what is necessary is just to let the part which is the 4-byte section low voltage of the read-out gate pulse e shown in the buffer memory write-in gate pulse c shown in drawing 3 (c), and drawing 3 (e) be high potential.
[0028] From the timing signal generator 1, the day interleave memory writing and the read-out gate pulse f which are shown in drawing 3 (f) are outputted to the address-data generator 3. In response to day interleave memory writing and the read-out gate pulse f, from the address-data generator 3, address data A and the R/W signal i are outputted to the day interleave memory 4, and a day interleave is performed.
[0029] Output-data j from the buffer memory 2 containing the dummy data shown in drawing 2 (c) is written in and read to the day interleave memory 4 by the address data A made in agreement in timing by day interleave memory writing and the read-out gate pulse, and the R/W signal i. Drawing 3 (g) Address data A, and the R/W signal i, the day interleave memory write-in data j and the read-out data k which expanded day interleave memory writing and the read-out gate pulse g to - (k) by 1 slot section, and were expanded to coincidence by 1 slot section are shown.
[0030] Also from drawing 3 , the data k with which the day interleave of [in front of 1 super frame] was first carried out so that clearly are read, and it becomes the order which writes in the present data j for carrying out a day interleave continuously. Moreover, the write-in data j become the same [the timing of write-in data and read-out data] by writing in the same address which read Data k. The read data k are data by which the day interleave was carried out, and the frame structure of them is the same as that of drawing 2 (c).
[0031] A day interleave is performed by the writing to the day interleave memory 4, and read-out actuation. Next, the address-data generator 3 is explained.
[0032] Before the detailed explanation about the address-data generator 3, the principle of address-data generating is explained based on drawing 4 , drawing 5 , and drawing 6 .
[0033] It is the example drawing 4 , drawing 5 , and drawing 6 explain a day interleave of nxm=4x5 when m sets the base unit (it is 203 bytes in the case of = BS digital broadcasting) of a data length, and n to m= 5 and n= 4 since it is easy although they were the depth (it is 8 (the number of the frames which constitute 1 super frame) in the case of = BS digital broadcasting) of an interleave to be.
[0034] The data into which address data were inputted by the lower berth are entered in the upper case of the day interleave matrix of drawing 4 (a), drawing 5 (a), (b), and (c). As shown in drawing 4 (a), data streams D [0], D [1], and D [2], D [3], --D [18], and D [19] are written in to address-data A [0], A [1], A [2], A [3], --A [18], and A [19]. This data is written in a longitudinal direction one by one, as shown in drawing 4 (c), as shown in drawing 4 (b), it is read to a lengthwise direction one by one, and an interleave is made.
[0035] This condition is shown in drawing 5 (a), and this condition is considered as the case of the address set number x= 0. This condition is A [0], A [1], A [2], A [3], A [4], A [5], ..., A [18], and A [19] one by one from the address-data generator 3.
** address data output -- having -- data streams D [0], D [1], and D [2], D [3], D [4], D [5], ..., D [18], and D [19]
The data streams D [0], D [5], and D [10] to boil and by which the receiving depth 4 was interleaved, D [15], D [1], D [6], ..., D [14], D [19]
It is ** writing ** rare ******.
[0036] In this case, the address data outputted from the address-data generator 3 are only increments, and call this a basic address set. The read-out address data from the day interleave memory 4 are the conditions D [0], D [1], and D [2] before the data stream after being read is interleaved, D [3], D [4], D [5], ..., D [18], and D [19].
From the address-data generator 3, they are A [0], A [4], A [8], A [12], A [16], A [1], ..., A [15], and A [19] one by one so that it may become.
** address data are outputted. This address set number x is set to 1.
[0037] The following data stream is written in the address position to which read-out was performed.

This data stream is D' [0], D' [5], D' [10], D' [15], D' [1], D' [6], ..., D' [14], and D' [19].
It comes out, and it is and drawing 5 (b) shows the condition that this data stream was written in.
[0038] for carrying out a day interleave similarly -- A [0], A [16], A [13], A [10], A [7], A [4], ..., A [3], and A [19]
** -- if addressing is carried out so that address data may be outputted like -- D' [0], D' [1], D' [2], D' [3], D' [4], D' [5], ..., D' [18], and D' [19]
** data are obtained. This condition is in the condition of the address set number x= 2.
[0039] moreover, the address position specified with the address data with which the order of these address data, i.e., data, was read -- one by one -- data D** [0], D** [5], D** [10], D** [15], D** [1], D** [6], ..., D** [14], and D** [19]
** writing ** -- A [0] of rare (drawing 5 (c)) and the address set number x= 3, A [7], A [14], A [2], A [9], A [16], ..., A [12], and A [19]
if data are read from the location specified with ** address data -- data D** [0], D** [1], D** [2], D** [3], D** [4], D** [5], ..., D** [18], and D** [19]
It ******.
[0040] The address number y corresponding to the address data of the proper assigned to the day interleave memory 4 in drawing 6 If transition of address data A to the address set number x which is the count which specified even the address number y corresponding to the count of read-out writing repeatedly is shown, for example, the address set number x= 2 is explained to an example It is shown address number [of the proper assigned to the day interleave memory 4] A [0], A [16], A [13], A [10], A [7], A [4], ..., that A [3] and A [19] are outputted from the address-data generator 3 as address data.
[0041] It is as following when the procedure of performing a day interleave is packed here.
a. Read by the address set number x= 0 (it omits most in the beginning), and write in by b. address set number x= 0. c. Read by the address set number x= 1, and it writes in by d. address set number x= 1. e. Read by the address set number x= 2, and it writes in by f. address set number x= 2. .. It reads by q. address set number x= 8, writes in by r. address set number x= 8, it becomes read-out by s. address set number x= 9 (= 0), and the data inputted into the address of the address data with which data were read are written in. Thus, it turns out that the address set number x patrols assignment of the address data in a day interleave of nxm=4x5 with the period of 9. The period of the address set number x describes this as a period X by 9. A period X= 0 is meaningless and X= 0 removes it.
[0042] Next, this addressing is general-formula-ized. If x and an address number are set to y and address data are set [the depth of a day interleave / n and the number of data of a base unit] to A for m and an address set number, they are address data A. x-th power of A=yxn modulo (nxm -1) (y!=nxm -1)
-- (one formula)
A=y (y=nxm -1) -- (two formulas)
It is alike and is specified more. In this case, a modulo b is the remainder of a-alpha b (natural number in which alpha contains 0), and when a is under b, a modulo b presupposes that it is a.
[0043] The period X of the address set number x is X= 9, as it was obtained by calculating x set to A= 1 in (1) type at the time of y= 1 and being described above in this case.
[0044] Although the example by drawing 4 , drawing 5 , and drawing 6 was general-formula-ized about the day interleave on a two-dimensional address matrix, it is applicable also to a day interleave of a BS-digital-broadcasting signal. Although an interleave of the depth 8 is performed in the direction of a frame between the same slots by the BS-digital-broadcasting signal, 203 bytes of main signal is assigned to one slot, and it can treat as that for which the two-dimensional matrices of 203 (cutting tool)x8 (frame) gathered 48 (slot). That is, the room for 1 super frame will be divided into 48, and a day interleave of 203x8 will be performed in each area.
[0045] With one gestalt of this operation, the memory matrix of 1 super frame is defined like drawing 7 . If it is referred to as m=203(cutting tool) xn=8(frame) xS=48 (slot), and the 1 case shift of the address is continuously incremented [in the direction of m] from the address 0 and carried out in the direction of n by the two-dimensional matrix of 203x8, it is incremented in the direction of m again and it sets like --, the last address of one slot will be set to 1623. moreover -- the direction of a slot -- the direction of the

1st slot to the 48th slot -- nxm= -- every [1624], offset shall be added and shall go
[0046] Also in this case, the period X of the address set number x is called for from x set to A= 1 in (1) type at the time of y= 1, and it is the period X= 180 of the address set number x.
[0047] The flow chart which shows the example of the address-data generator 3 to drawing 8 , and shows the operation to drawing 9 and drawing 10 is shown.
[0048] The address-data generator 3 is equipped with the MODEYURO operation part 52 which collaborates with the slot number detecting element 51, and the strobe pulse generating section 50 and the slot number detecting element 51 which collaborates with the strobe pulse generating section 50 and the strobe generating section 50, and specifies the number of a slot, performs a MODEYURO operation, and sends out address data as shown in drawing 8 . Here, it is m= 203 (byte count of the main signal in one slot), n= 8 (depth of a day interleave), S= 48 (the number of slots in one frame), F= 8 (it is the frame number which constitutes 1 super frame, and is F=n=8), and X= 180 (period of the count x of an address set). the MODEYURO operation part 52 except the adder 70 which carries out a postscript here -- an offset value -- counting -- it corresponds to a means.
[0049] The day interleave writing to which the strobe pulse generating section 50 is outputted from the timing signal generator 1, m ** counter 53 with which a read-out gate pulse is supplied and this day interleave writing and a read-out gate pulse carry out counting of the clock pulse in response to the clock pulse of high potential by which a period output is carried out, S ** counter 54 which performs counting of the carry output of m ** counter 53, F ** counter 55 which performs counting of the carry output of S ** counter 54, X ** counter 56 which performs counting of the carry output of F ** counter 55, It consists of a decoder 57 which generates a strobe pulse in response to the enumerated data mcnt of m ** counter 53, the enumerated data Scnt of S ** counter 54, the enumerated data Fcnt of F ** counter 55, and the enumerated data xcnt of X ** counter 56.
[0050] Since the increment of the enumerated data of S ** counter 54 is carried out whenever m ** counter 53 carries out counting of the clock pulse 203 times from 0, S ** counter 54 will have detected the slot number. In the slot number detecting element 51, it consists of a multiplier 58 doubled in response to the enumerated data of S ** counter 54 (nxm), and the initiation address data 0, 1624, 3248, --, 76328 of the slot number will be generated based on the enumerated data of S ** counter 54. The after-mentioned data A0 are added to this output from the slot number detecting element 51, and address data A are obtained.
[0051] The MODEYURO operation part 52 A offset register 60 The setter 59 and strobe pulse sa which are initialized to the set point 1 The adder 62 adding ****** of A offset register 60 with which popularity is won and the number of ** of the ****** of R offset register 61 is carried out, R offset register 61 which carries out the number of ** of the address data A0 in response to a strobe pulse sb, and address data A0 and A offset register 60, The comparator 64 which compares the addition output of an adder 62 with the set point (nxm) of a setter 63, The value which subtracted the set point (nxm -1) of a setter 65 from the addition output of an adder 62 based on the output of the comparator 64 at the time of (the set point (nxm) of the addition output >= setter 63 of an adder 62) is outputted as address-data A**. and (set point of the addition output >= setter 63 of an adder 62 (nxm)) -- it is not -- the time -- a comparator 64 -- with the subtractor 66 which outputs the addition output of an adder 62 as address-data A** based on an output The Amcnt register 67 which makes ****** address-data A** outputted from a subtractor 66 in response to a strobe pulse sc, The selector 68 which chooses one side of address-data A** outputted from a subtractor 66, and ****** of the Amcnt register 67 by the selection pulse sp, It has the adder 70 adding the latch 69 who consists of DF/F which one clock pulse makes carry out period delay of address-data A' outputted from a selector 68, and the address data A0 and the output of a multiplier 58 which were latched, and let the output of an adder 70 be address data A.
[0052] The strobe pulse sa to A offset register 60 is outputted synchronizing with the carry output of F ** counter 55. However, in xcnt=X -1, the number of ** of 1 is carried out, and when it is xcnt!=X -1, the number of ** of ****** Rofset of R offset register 61 is carried out. The enumerated data Fcnt of F ** counter 53 are outputted when, as for the strobe pulse sb to R offset register 61, the enumerated data mcnt of 0 and m ** counter 53 are set to n by the enumerated data Scnt of 0 and S ** counter 52. The

enumerated data Scnt of S ** counter 52 are 0, and the strobe pulse sc to the Amcnt register 67 is outputted when the enumerated data mcnt of m ** counter 53 are set to 0. The selection pulse sp to a selector 68 is outputted when it becomes enumerated-data mcnt=m -1 of m ** counter 53, and enumerated-data Scnt!=S -1 of S ** counter 52, and ****** of the Amcnt register 67 is chosen.
[0053] The value and address data A0 by which the number of ** was carried out to A offset register with the adder 62 are added, and an addition result is sent out to a comparator 64 and a subtractor 66. Address data A0 are the address data on the two-dimensional matrix of 203x8, and the addition result of the value (that is, offset to the direction of a slot) and address data A0 which doubled the enumerated data Scnt of S ** counter 54 which counts the number of slots nxm with the multiplier 58 serves as address data A.
[0054] a comparator 64 outputs subtraction directions to a subtractor 66, when the addition output of an adder 62 becomes the above (nxm (= 1624)), and a subtractor 66 is set as a setter 65 from the addition output from an adder 62 in response to subtraction directions -- **** (nxm -1) -- it subtracts. Moreover, when the addition output of an adder 62 is not above (nxm (= 1624)), it does not subtract, but the addition output of an adder 62 is outputted from a subtractor 66 as it is.
[0055] Address-data A** in the generating time of a strobe pulse sc is made the Amcnt register 67 the number of **, and it gets down, and when a selector 68 receives a select signal sp, ****** A** of the Amcnt register 67 is selected and outputted. The output from a selector 68 is made into address-data A'. Address-data A' is latched by latch 69 and uses a latch output as address data A0. Moreover, in response to a strobe pulse sa, as for R offset register 61, the number of ** of the data A0 in the time is carried out. Moreover, ****** of R offset register 61 is outputted to A offset register 60, and the number of ** is carried out to A offset register 60 in response to a strobe pulse sa.
[0056] Although m ** counter 53, S ** counter 54, F ** counter 55, X ** counter 56, and the latch 69 are operating by the common clock pulse, actuation is suspended when day interleave memory writing and a read-out gate pulse are low voltage.
[0057] An operation of the address-data generator 3 is explained based on the flow chart of drawing 9 and drawing 10 .
[0058] If a day interleave is started, ****** Aofset of A offset register 60 will be initialized by 1, and it will be initialized by 0 (step S1)., the enumerated data xcnt x, i.e., the address set number, of X ** counter 56 Moreover, the enumerated data mcnt of m ** counter 53, the enumerated data Scnt of S ** counter 54, and the enumerated data Fcnt of a counter F54 are initialized by 0, latch 69 is also initialized, and address data A0 are also initialized (step S2). Although the number of ** of the data A** at this time is carried out to the Amcnt register 67, the number of ** of 0 will be carried out in this case (step S3). Moreover, since it becomes quantity potential when, as for a strobe pulse sc, the enumerated data Scnt of 0 and S ** counter 52 are set to 0 by the enumerated data mcnt of m ** counter 53, the number of ** to the Amcnt register 67 will be performed for every increment of F ** counter 55.
[0059] ****** to the Amcnt register 67 outputted through the selector 68 is latched by latch 69, and address data A0 decide it (step S4). It is confirmed from a decoder 57 whether to be enumerated-data Fcnt=0 of F ** counter 55, enumerated-data Scnt=0 of S ** counter 54, and enumerated-data mcnt=n=8 of m ** counter 53 (step S5). In step S5, when distinguished from enumerated-data Fcnt=0 of F ** counter 55, enumerated-data Scnt=0 of S ** counter 54, and enumerated-data mcnt=n=8 of m ** counter 53, a strobe pulse sb is outputted, the number of ** of the address data A0 is carried out to R offset register 61 (step S6), and step S7 is performed. However, at this time, since it is enumerated-data mcnt=0 of m ** counter 53, step S7 is performed from step S5.
[0060] Although not illustrated in drawing 9 following step S7, the increment of the enumerated data mcn of m ** counter 53 is carried out, and, subsequently step S8 is performed until the enumerated data mcnt of m ** counter 53 become enumerated-data mcnt=m -1 (= 202) in step S7. ****** by which the number of ** is carried out to address data A0 and A offset register 60 with the adder 62 in step S8 is added (step S8). When addition output A**' of an adder 62 is above (nxm (= 1624)), (nxm -1 (= 1623)) is subtracted from (step S9) and addition output A**', and it performs from step S4 (step S10). When addition output A**' of an adder 62 is not above (nxm (= 1624)), it performs from step S4 following

step S9.
[0061] When the actuation so far is tested by comparison to the general formula of said addressing, n of ****** of A offset register 60 is equal to the x-th power (when the x-th power of n exceeds (nxm -1), it is equal to the remainder when repeating and subtracting (nxm -1)), and the x-th power of yxn is equal to the accumulation of the x-th power of n. Moreover, since data A**' does not exceed the twice of (nxm -1), the MODEYURO operation of (nxm -1) can simplify a configuration by subtracting (nxm -1), when (nxm -1) is exceeded. In the last address where data A**' becomes equal to (nxm -1), if (nxm -1) is subtracted, it will be set to 0 and fault will be caused.
[0062] However, that A**' becomes equal to (nxm -1) can avoid this by changing, if (nxm -1) is subtracted from it being only the last address when (nxm) is exceeded for the conditions of subtraction. This is equivalent to having simplified the conditions made into A=y in y=nxm -1 of the general formula of said addressing.
[0063] When the enumerated data mcnt of m ** counter 53 are set to m-1 (= 202), the step of conditional branching based on the enumerated data Scnt of S ** counter 54 is performed (step S11). Step S12 is performed until the enumerated data Scnt of S ** counter 54 are set to S-1 (= 47), and it performs repeatedly following step S12 from step S4. At step S12, the increment of the enumerated data Scnt of S ** counter 54 is carried out, the enumerated data mcnt of m ** counter 53 are reset, and ****** of the Amcnt register 67 is outputted as address-data A' (step S12). That is, ****** of the Amcnt register 67 is chosen by the selector 68. This actuation is for being in a frame and making equal initial value of the address data A of each slot.
[0064] For example, in the 1st frame, the address data A0 of each slot start 0, and it begins from 203 in the 2nd frame. Therefore, in the 2nd frame, whenever a slot replaces, it is necessary to load 203 to address data A0. Since it is enumerated-data Fcnt=0 of F ** counter 55, i.e., the 1st frame, at present, 0 by which the number of ** was carried out to the Amcnt register 67 for every increment of a slot will be loaded. The above-mentioned actuation is repeated until the enumerated data Scnt of S ** counter 54 are set to S-1 (= 47).
[0065] When the enumerated data Scnt of S ** counter 54 are set to S-1 (= 47), the conditional-branching step based on the enumerated data Fcnt of F ** counter 55 is performed (step S13). When not fulfilling enumerated-data Fcnt=F-1 of F ** counter 55 in step S13, step S14 is performed, the increment of the enumerated data Fcnt of F ** counter 55 is carried out, and reset of the enumerated data Scnt of S ** counter 54 and the enumerated data mcnt of m ** counter 53 is performed (step S14). Then, A offset registerA0 accumulates to 60 (step S15). This is because the initial value of the address data A0 at the time of frame modification turns into the next value of the data A0 of the final value of a front frame.
[0066] That is, when the address set number x is 0, the last address data A0 of the 1st frame are 202, and since ****** of A offset register 60 is 1, the head of two frames is set to 202+1=203. Moreover, as a result of step S15, step S16 is performed, data A'>= (nxm) is checked, as a result of step S16, step S17 is performed alternatively and, subsequently step S3 is performed. What (nxm -1) is subtracted for when data A' exceeds (nxm) (step S17) is the same as that of the aforementioned case. Furthermore, this result serves as a value loaded whenever the number of ** is carried out to the Amcnt register 67 by step S3 and a slot is changed by it.
[0067] When the enumerated data Fcnt of F ** counter 55 become F-1 (= 7) in step S13, at this time, the day interleave for 1 super frame is completed. When the address set number x has not reached x=X -1 (= 179) by conditional branching (step S20) based on the enumerated data xcnt of X ** counter 56, step S21 is performed and the number of ** of the ****** of R offset register 61 by which the number of ** was carried out in step S6 is carried out to A offset register 60 (step S21). Furthermore, the increment of the address set number x is carried out (step S22).
[0068] this actuation -- the general formula of said addressing carried out -- and (one formula) (two formulas) it explains.
[0069] ****** of A offset register 60 is the address data A (value of the x-th power of A=1xn) of the x-th power of n, i.e., the case of y= 1, (although it is equal (like the above)). Are equal to the remainder

when repeating subtraction by (nxm -1), when the value of the x-th power of n exceeds (nxm -1). ****** Aofset' of A offset register 60 of the following address set becomes the x-th power of x-th power xn=8x[of ** (x+1) =1xn] n of 1xn similarly, and this is equal to the address data A in y= 8. putting in another way -- if -- current -- y -- = -- eight -- address data -- A -- memorizing -- if -- this -- a degree -- the address -- a set -- a number -- x -- A -- offset -- a register -- 60 -- ****** -- it is -- Aofset -- ' -- becoming -- count -- a circuit -- being omissible -- ******** . Since the address data A at the time of y=mcnt=n=8 were memorized to R offset register 61 by step S5 and step S6, before progressing to the following address set, this is written in A offset register 60. Moreover, all are initialized when the enumerated data xcnt of X ** counter 56 are set to X-1 (= 179).

[0070] Some address data A generated by one gestalt of this operation are shown in drawing 11 and drawing 12 . From the relation of space, the address set number x showed even 17 and the address number y showed even 50.

[0071] According to the day interleave circuit which starts one gestalt of this operation as mentioned above As opposed to the address data A to the day interleave memory 4 which made it generate by the address-data generator 3 A lead (R), The utilization ratio of memory is raised by being carried out by a lead preceding rather than a light, and writing data in the address which became an opening by having read data like a light (W), a lead (R), a light (W), and ....

[0072] On the other hand, two address-data generators are formed, for example, and one is read, and it can carry out only to address-data generating, one can be written in, and it can read to a high speed per super frame as only for address data. In this case, address data must be the same address data. For example, according to the timing shown in drawing 3 , if it reads and writes [both] in and 203 byte processings are carried out, it is a repetition called a 4-byte section pause, but it is also possible to read only read-out continuously, without carrying out 4 bytes of pause.

[0073]

[Effect of the Invention] According to the day interleave circuit which starts this invention as explained above, a day interleave can be performed now by the memory of the memory capacity for 1 super frame, and the effectiveness that components mark and components cost fall is acquired. Moreover, when it integrated-circuit-izes, the gate number can be reduced compared with the former, and a chip area can contract sharply.

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] It is a day interleave circuit in a BS-digital-broadcasting receiver. Set the number of the main signals in 1 slot to m, and the depth of a day interleave is set to n. The address number of the proper assigned to the memory for a day interleave is set to y. When the address data which specify the R/W address position of data are set to A and it presupposes that a modulo b is the remainder of a-alpha b (natural number in which alpha contains 0), It is the x-th power of A=yxn at the time of (y!=nxm -1). It is referred to as modulo (nxm -1). It is the x-th power of A=yxn about the address set number x which is the count which considered as A=y and specified even the address number y repeatedly at the time of (y=nxm -1). It is referred to as x set to A= 1 in modulo (nxm -1) at the time of y= 1. And it has an address-data generating means to generate the address data A made into A= (x-th power of yxn) when the value of the x-th power of yxn is under a value of (nxm -1). The day interleave circuit characterized by writing in the following main signal which reads the main signal memorized by the address position of the memory specified with the address data generated by the address generation means, and an interleave is carried out to this address position, and is inputted into it.
[Claim 2] m ** counter which carries out counting of the number of the main signals into which an address-data generating means is inputted in a day interleave circuit according to claim 1, S ** counter which carries out counting of the carry of m ** counter, and the multiplier which carries out the multiplication of (nxm) to the enumerated data of S ** counter, When a main signal value amounts to (m-1), carry out 1 case shift in the direction of n, and counting of the main signal is carried out in the direction of a slot. the direction of a slot -- the number of the main signals -- counting -- carrying out -- counting -- the offset value to which enumerated data carry out counting of it repeatedly similarly until at least order reaches (nxm) -- counting -- a means, the output of a multiplier, and an offset value -- counting -- the day interleave circuit characterized by having an addition means to add counting of a means and using the output of an addition means as address data A.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the day interleave circuit used for a BS-digital-broadcasting receiver.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] 8x203 bytes of block interleave is performed per cutting tool, and the interleave is performed between slots with the same slot number of each frame in the direction of a super frame as the interleave method in a BS-digital-broadcasting receiver is already learned.
[0003] Here, the MPEG 2-TS packet of the main signal of a BS-digital-broadcasting signal consists of one slot formed by 1 byte of transmission multiplex control (TMCC (Transmission andMultiplexing Cofiguration Control)) signal 204 bytes, in order to show 203 bytes, a synchronizing signal, a modulation technique, error correcting system containing 16 bytes of parity for outside digital-error correction, etc., it constitutes one frame from 48 slots, and is using eight frames as 1 super frame.
[0004] In order to carry out the day interleave of the data interleaved as mentioned above, the memory which has the storage capacity for 2 super frame was required. For this reason, the memory of the storage capacity which also amounts to a maximum of 155904 bytes (=203(cutting tool) x48(slot) x8 frame x2 (super frame)) is required.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to the day interleave circuit which starts this invention as explained above, a day interleave can be performed now by the memory of the memory capacity for 1 super frame, and the effectiveness that components mark and components cost fall is acquired. Moreover, when it integrated-circuit-izes, the gate number can be reduced compared with the former, and a chip area can contract sharply.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, when a day interleave circuit was constituted using the memory of the memory capacity which attains to 2 super frame like before, when a day interleave circuit was integrated-circuit-ized, the gate number increased, and also there was a trouble that a chip area will become large.
[0006] This invention aims at offering the day interleave circuit where there is little memory capacity and it ends.

[Translation done.]

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MEANS

[Means for Solving the Problem] The day interleave circuit concerning this invention is a day interleave circuit in a BS-digital-broadcasting receiver. Set the number of the main signals in 1 slot to m, and the depth of a day interleave is set to n. The address number of the proper assigned to the memory for a day interleave is set to y. When the address data which specify the R/W address position of data are set to A and it presupposes that a modulo b is the remainder of a-alpha b (natural number in which alpha contains 0), It is the x-th power of A=yxn at the time of (y!=nxm -1). It is referred to as modulo (nxm -1). It is the x-th power of A=yxn about the address set number x which is the count which considered as A=y and specified even the address number y repeatedly at the time of (y=nxm -1). It is referred to as x set to A= 1 in modulo (nxm -1) at the time of y= 1. And it has an address-data generating means to generate the address data A made into A= (x-th power of yxn) when the value of the x-th power of yxn is under a value of (nxm -1). The main signal memorized by the address position of the memory specified with the address data generated by the address generation means is read, and it is characterized by writing in the following main signal which an interleave is carried out to this address position, and is inputted into it.
[0008] In the day interleave circuit concerning this invention, the main signal memorized by the address position of the memory specified with the address data A generated by the address generation means is read. Since the following main signal which an interleave is carried out [the signal] to the address position which became an opening substantially by this read-out, and is inputted into it is written in, when the day interleave could be performed with the memory capacity of the memory for a day interleave, the memory capacity of the memory for a day interleave is the memory of one half of memory capacity, and ends to the memory of the memory capacity of 2 super frame needed conventionally and it integrated-circuit-izes, there will be little need area and it will end.
[0009] m ** counter which carries out counting of the number of the main signals into which an address-data generating means is inputted in the day interleave circuit concerning this invention, S ** counter which carries out counting of the carry of m ** counter, and the multiplier which carries out the multiplication of (nxm) to the enumerated data of S ** counter, When a main signal value amounts to (m-1), carry out 1 case shift in the direction of n, and counting of the main signal is carried out in the direction of a slot. the direction of a slot -- the number of the main signals -- counting -- carrying out -- counting -- the offset value to which enumerated data carry out counting of it repeatedly similarly until at least order reaches (nxm) -- counting -- a means, the output of a multiplier, and an offset value -- counting -- it has an addition means to add counting of a means, and is characterized by using the output of an addition means as address data A.
[0010] A day interleave is performed by reading the main signal from the address position of memory specified with the address data outputted from an address generation means, and being written in.
[0011]
[Embodiment of the Invention] Hereafter, the gestalt of operation of the day interleave circuit concerning this invention explains.
[0012] Drawing 1 is the block diagram showing the configuration of the day interleave circuit concerning one gestalt of operation of this invention. As for the day interleave circuit concerning one

gestalt of operation of this invention, trellis sign method (trellis sign method is hereafter described as TC) 8PSK (rate r=of coding 2/3) has illustrated the case where the method type QPSK of 46 slots, convolutional-code-izing, and blowout CHADO encoding (rate r=of coding 1/2) is one slot.
[0013] Drawing 3 (a) shows the super frame pulse a outputted synchronizing with each super frame. The inner sign decode data b shown in drawing 3 (b) decoded and cutting-tool-ized by the trellis and the Viterbi decoder which are a decoder to the output by which received the BS-digital-broadcasting signal and inner sign decode was carried out (cutting tool unit), i.e., a trellis sign, and a convolutional code are outputted synchronizing with the super frame pulse a. The inner sign decode data b are written in buffer memory 2 in response to the write-in gate pulse c shown in drawing 3 (c) outputted from the timing signal generator 1 which received the super frame timing signal and the transmission-mode signal.
[0014] 203 bytes of main signal is written in the buffer memory 2 which consists of FIFO by the write-in gate pulse c, and this writing is memorized. It dissociates, and a synchronizing signal, a TMCC signal, and a burst symbol signal are not written in buffer memory 2, but non-data are written in at this period. In drawing 3 (c), 4 bytes of notation shows the burst symbol period.
[0015] Here, depending on a modulation technique and the rate of coding, the data rate of the data rate of the cutting-tool-ized data is 1/2 with 1, then a QPSK sign (rate r=of coding 1 / 2 (rate r=of coding 1/2 may omit hereafter)) about the data rate of a TC8PSK sign (rate r=of coding 2 / 3 (rate r=of coding 2/3 may omit hereafter)). Therefore, with this 1 gestalt, it is the case where 8PSK signs are 46 slots and a QPSK sign is one slot, the information bit transmission efficiency of a QPSK sign is 1/2 in the case of 8PSK signs, and since the modulation of symbol rate regularity is carried out, a transmission slot turns into two slots and turns into 48 slots at one frame.
[0016] Moreover, with a BPSK sign (rate r=of coding 1 / 2 (rate r=of coding 1/2 may omit hereafter)), a data rate is 1/4. Moreover, the synchronizing signals and the TMCC signal sections which are transmitted by BPSK (rate r=of coding 1/2) are one fourth of data rates to the data rate of TC8PSK, 4 bytes of burst symbol signal is transmitted by QPSK (rate r=of coding 1/2), and the data rates of a burst symbol signal are one half of data rates.
[0017] In response to the write-in gate pulse c outputted from the timing signal generator 1, it is as the performing [a TMCC signal and a burst symbol signal are separated from the main signal in the case of writing, and / the writing to buffer memory 2] above to the buffer memory 2 of 203 bytes of main signal.
[0018] The inner sign decode output b written in buffer memory 2 From the generating stage of the read-out start pulse d shown in drawing 3 (d) which set predetermined time difference from the super frame pulse shown in drawing 3 (a) In response to the read-out gate pulse e shown in drawing 3 (e) outputted from the timing signal generator 1, period read-out of a TMCC signal and a burst symbol signal is stopped substantially. 203 bytes of main signal j (a publication of 203 bytes of cutting tool may be omitted hereafter) is burstily read from buffer memory 2 at a fixed rate. Furthermore, the day interleave writing and the read-out gate pulse f which are shown [drawing 3 (f), (a part being expanded to drawing 3 (g) and it being shown), and] in the address-data generator 3 from the timing signal generator 1 are outputted.
[0019] The R/W signal i shown in the address data A shown in drawing 3 (h) from day interleave memory writing and the address-data generator 3 which received the read-out gate pulse f, and drawing 3 (i) is outputted to the day interleave memory 4. 203 bytes of main signal j shown in drawing 3 (j) is written in the day interleave memory 4 one by one. Based on read-out addressing, a day interleave is performed on the occasion of read-out from the day interleave memory 4, and 203 bytes of main signal k shown in drawing 3 (k) by which the day interleave was carried out is outputted from the day interleave memory 4.
[0020] The R/W signal i is read at the time of high potential, directions are performed, when it is low voltage, it writes in, directions are performed and the main signal supplied to the address with which the main signal j was read by addressing by address data A at the degree is written in.
[0021] Next, based on drawing 2 , it explains to a detail further. Drawing 2 shows the data frame configuration for every processing process in one gestalt of this operation.

[0022] Drawing 2 (a) shows the inner sign decode data b supplied to buffer memory 2. The inner sign decode data b shown in drawing 2 (a) are a TC8PSK signal about 46 slots. The frame structure for 1 super frame in the case of transmitting one slot by the QPSK signal (rate r=of coding 1/2) is shown. 12 bytes of synchronization and a TMCC signal are followed. 203 bytes of main signal of TC8PSK, 4 bytes of null section, 203 bytes of main signal equivalent to a burst symbol signal, 4 bytes of null section equivalent to a burst symbol signal, --, 203 bytes of main signal of QPSK (rate r=of coding 1/2), One frame consists of 4 bytes of the null sections equivalent to a burst symbol signal, and 1 super frame consists of eight frame [0th] - frame [7th] frames.
[0023] Only the section of high potential [gate pulse / this] is written in buffer memory 2 by the write-in gate pulse c, and the data stream of the inner sign decode data b shown in drawing 2 (a) is memorized. As shown in drawing 2 (b), the main signal, i.e., a synchronizing signal, a TMCC signal, and signals other than the burst symbol signal section are written in buffer memory 2.
[0024] In the timing signal generator 1, fixed time delay was carried out in response to the super frame pulse a, and it reads, and start signal d is generated, it reads by this timing, and a gate pulse e is outputted. In response to the read-out gate pulse e, read-out is performed at a fixed rate from buffer memory 2. Let a read-out rate be the rate of 8PSK which is a base rate.
[0025] the read-out gate pulse e -- 48 bytes of synchronization, and a TMCC signal section pause -- carrying out -- 203 bytes -- reading -- 4 bytes -- stopping -- 203 bytes -- reading -- 4 bytes -- stopping -- and 203 bytes -- stopping -- 4 bytes -- stopping -- ** -- ** It is because the data rate writes in that a synchronization and the TMCC signal section become 48 bytes, and it was 1/4, so it sometimes becomes with the 4 times (12 byte x4=48) at the time of read-out.
[0026] Although the transmission slots are two slots since it is 1/2 in the case of a TS8PSK sign and, as for having considered as the 203-byte pause at the last, the modulation of symbol rate regularity is carried out, as for the information bit transmission efficiency of the QPSK sign of the main signal, it is for becoming 203 bytes and inserting dummy data in this part by inner sign decode. Drawing 2 (c) shows signs that dummy data was inserted in the part considered as the 203-byte pause.
[0027] In addition, although a burst symbol signal is not written in buffer memory 2 here, a burst signal may also be written in with the main signal, and you may read. In this case, what is necessary is just to let the part which is the 4-byte section low voltage of the read-out gate pulse e shown in the buffer memory write-in gate pulse c shown in drawing 3 (c), and drawing 3 (e) be high potential.
[0028] From the timing signal generator 1, the day interleave memory writing and the read-out gate pulse f which are shown in drawing 3 (f) are outputted to the address-data generator 3. In response to day interleave memory writing and the read-out gate pulse f, from the address-data generator 3, address data A and the R/W signal i are outputted to the day interleave memory 4, and a day interleave is performed.
[0029] Output-data j from the buffer memory 2 containing the dummy data shown in drawing 2 (c) is written in and read to the day interleave memory 4 by the address data A made in agreement in timing by day interleave memory writing and the read-out gate pulse, and the R/W signal i. Drawing 3 (g) Address data A, and the R/W signal i, the day interleave memory write-in data j and the read-out data k which expanded day interleave memory writing and the read-out gate pulse g to - (k) by 1 slot section, and were expanded to coincidence by 1 slot section are shown.
[0030] Also from drawing 3 , the data k with which the day interleave of [in front of 1 super frame] was first carried out so that clearly are read, and it becomes the order which writes in the present data j for carrying out a day interleave continuously. Moreover, the write-in data j become the same [the timing of write-in data and read-out data] by writing in the same address which read Data k. The read data k are data by which the day interleave was carried out, and the frame structure of them is the same as that of drawing 2 (c).
[0031] A day interleave is performed by the writing to the day interleave memory 4, and read-out actuation. Next, the address-data generator 3 is explained.
[0032] Before the detailed explanation about the address-data generator 3, the principle of address-data generating is explained based on drawing 4 , drawing 5 , and drawing 6 .

[0033] It is the example drawing 4 , drawing 5 , and drawing 6 explain a day interleave of nxm=4x5 when m sets the base unit (it is 203 bytes in the case of = BS digital broadcasting) of a data length, and n to m= 5 and n= 4 since it is easy although they were the depth (it is 8 (the number of the frames which constitute 1 super frame) in the case of = BS digital broadcasting) of an interleave to be.
[0034] The data into which address data were inputted by the lower berth are entered in the upper case of the day interleave matrix of drawing 4 (a), drawing 5 (a), (b), and (c). As shown in drawing 4 (a), data streams D [0], D [1], and D [2], D [3], --D [18], and D [19] are written in to address-data A [0], A [1], A [2], A [3], --A [18], and A [19]. This data is written in a longitudinal direction one by one, as shown in drawing 4 (c), as shown in drawing 4 (b), it is read to a lengthwise direction one by one, and an interleave is made.
[0035] This condition is shown in drawing 5 (a), and this condition is considered as the case of the address set number x= 0. This condition is A [0], A [1], A [2], A [3], A [4], A [5], ..., A [18], and A [19] one by one from the address-data generator 3.
** address data output -- having -- data streams D [0], D [1], and D [2], D [3], D [4], D [5], ..., D [18], and D [19]
The data streams D [0], D [5], and D [10] to boil and by which the receiving depth 4 was interleaved, D [15], D [1], D [6], ..., D [14], D [19]
It is ** writing ** rare ******.
[0036] In this case, the address data outputted from the address-data generator 3 are only increments, and call this a basic address set. The read-out address data from the day interleave memory 4 are the conditions D [0], D [1], and D [2] before the data stream after being read is interleaved, D [3], D [4], D [5], ..., D [18], and D [19].
From the address-data generator 3, they are A [0], A [4], A [8], A [12], A [16], A [1], ..., A [15], and A [19] one by one so that it may become.
** address data are outputted. This address set number x is set to 1.
[0037] The following data stream is written in the address position to which read-out was performed. This data stream is D' [0], D' [5], D' [10], D' [15], D' [1], D' [6], ..., D' [14], and D' [19].
It comes out, and it is and drawing 5 (b) shows the condition that this data stream was written in.
[0038] for carrying out a day interleave similarly -- A [0], A [16], A [13], A [10], A [7], A [4], ..., A [3], and A [19]
** -- if addressing is carried out so that address data may be outputted like -- D' [0], D' [1], D' [2], D' [3], D' [4], D' [5], ..., D' [18], and D' [19]
** data are obtained. This condition is in the condition of the address set number x= 2.
[0039] moreover, the address position specified with the address data with which the order of these address data, i.e., data, was read -- one by one -- data D** [0], D** [5], D** [10], D** [15], D** [1], D** [6], ..., D** [14], and D** [19]
** writing ** -- A [0] of rare (drawing 5 (c)) and the address set number x= 3, A [7], A [14], A [2], A [9], A [16], ..., A [12], and A [19]
if data are read from the location specified with ** address data -- data D** [0], D** [1], D** [2], D** [3], D** [4], D** [5], ..., D** [18], and D** [19]
It ******.
[0040] The address number y corresponding to the address data of the proper assigned to the day interleave memory 4 in drawing 6 If transition of address data A to the address set number x which is the count which specified even the address number y corresponding to the count of read-out writing repeatedly is shown, for example, the address set number x= 2 is explained to an example It is shown address number [of the proper assigned to the day interleave memory 4] A [0], A [16], A [13], A [10], A [7], A [4], ..., that A [3] and A [19] are outputted from the address-data generator 3 as address data.
[0041] It is as following when the procedure of performing a day interleave is packed here.
a. Read by the address set number x= 0 (it omits most in the beginning), and write in by b. address set number x= 0. c. Read by the address set number x= 1, and it writes in by d. address set number x= 1. e. Read by the address set number x= 2, and it writes in by f. address set number x= 2. .. It reads by q.

address set number x= 8, writes in by r. address set number x= 8, it becomes read-out by s. address set number x= 9 (= 0), and the data inputted into the address of the address data with which data were read are written in. Thus, it turns out that the address set number x patrols assignment of the address data in a day interleave of nxm=4x5 with the period of 9. The period of the address set number x describes this as a period X by 9. A period X= 0 is meaningless and X= 0 removes it.
[0042] Next, this addressing is general-formula-ized. If x and an address number are set to y and address data are set [the depth of a day interleave / n and the number of data of a base unit] to A for m and an address set number, they are address data A. x-th power of A=yxn modulo (nxm -1) (y!=nxm -1)
-- (one formula)
A=y (y=nxm -1) -- (two formulas)
It is alike and is specified more. In this case, a modulo b is the remainder of a-alpha b (natural number in which alpha contains 0), and when a is under b, a modulo b presupposes that it is a.
[0043] The period X of the address set number x is X= 9, as it was obtained by calculating x set to A= 1 in (1) type at the time of y= 1 and being described above in this case.
[0044] Although the example by drawing 4 , drawing 5 , and drawing 6 was general-formula-ized about the day interleave on a two-dimensional address matrix, it is applicable also to a day interleave of a BS-digital-broadcasting signal. Although an interleave of the depth 8 is performed in the direction of a frame between the same slots by the BS-digital-broadcasting signal, 203 bytes of main signal is assigned to one slot, and it can treat as that for which the two-dimensional matrices of 203 (cutting tool)x8 (frame) gathered 48 (slot). That is, the room for 1 super frame will be divided into 48, and a day interleave of 203x8 will be performed in each area.
[0045] With one gestalt of this operation, the memory matrix of 1 super frame is defined like drawing 7 . If it is referred to as m=203(cutting tool) xn=8(frame) xS=48 (slot), and the 1 case shift of the address is continuously incremented [in the direction of m] from the address 0 and carried out in the direction of n by the two-dimensional matrix of 203x8, it is incremented in the direction of m again and it sets like --, the last address of one slot will be set to 1623. moreover -- the direction of a slot -- the direction of the 1st slot to the 48th slot -- nxm= -- every [1624], offset shall be added and shall go
[0046] Also in this case, the period X of the address set number x is called for from x set to A= 1 in (1) type at the time of y= 1, and it is the period X= 180 of the address set number x.
[0047] The flow chart which shows the example of the address-data generator 3 to drawing 8 , and shows the operation to drawing 9 and drawing 10 is shown.
[0048] The address-data generator 3 is equipped with the MODEYURO operation part 52 which collaborates with the slot number detecting element 51, and the strobe pulse generating section 50 and the slot number detecting element 51 which collaborates with the strobe pulse generating section 50 and the strobe generating section 50, and specifies the number of a slot, performs a MODEYURO operation, and sends out address data as shown in drawing 8 . Here, it is m= 203 (byte count of the main signal in one slot), n= 8 (depth of a day interleave), S= 48 (the number of slots in one frame), F= 8 (it is the frame number which constitutes 1 super frame, and is F=n=8), and X= 180 (period of the count x of an address set). the MODEYURO operation part 52 except the adder 70 which carries out a postscript here -- an offset value -- counting -- it corresponds to a means.
[0049] The day interleave writing to which the strobe pulse generating section 50 is outputted from the timing signal generator 1, m ** counter 53 with which a read-out gate pulse is supplied and this day interleave writing and a read-out gate pulse carry out counting of the clock pulse in response to the clock pulse of high potential by which a period output is carried out, S ** counter 54 which performs counting of the carry output of m ** counter 53, F ** counter 55 which performs counting of the carry output of S ** counter 54, X ** counter 56 which performs counting of the carry output of F ** counter 55, It consists of a decoder 57 which generates a strobe pulse in response to the enumerated data mcnt of m ** counter 53, the enumerated data Scnt of S ** counter 54, the enumerated data Fcnt of F ** counter 55, and the enumerated data xcnt of X ** counter 56.
[0050] Since the increment of the enumerated data of S ** counter 54 is carried out whenever m ** counter 53 carries out counting of the clock pulse 203 times from 0, S ** counter 54 will have detected

the slot number. In the slot number detecting element 51, it consists of a multiplier 58 doubled in response to the enumerated data of S ** counter 54 (nxm), and the initiation address data 0, 1624, 3248, --, 76328 of the slot number will be generated based on the enumerated data of S ** counter 54. The after-mentioned data A0 are added to this output from the slot number detecting element 51, and address data A are obtained.

[0051] The MODEYURO operation part 52 A offset register 60 The setter 59 and strobe pulse sa which are initialized to the set point 1 The adder 62 adding ****** of A offset register 60 with which popularity is won and the number of ** of the ****** of R offset register 61 is carried out, R offset register 61 which carries out the number of ** of the address data A0 in response to a strobe pulse sb, and address data A0 and A offset register 60, The comparator 64 which compares the addition output of an adder 62 with the set point (nxm) of a setter 63, The value which subtracted the set point (nxm -1) of a setter 65 from the addition output of an adder 62 based on the output of the comparator 64 at the time of (the set point (nxm) of the addition output >= setter 63 of an adder 62) is outputted as address-data A**. and (set point of the addition output >= setter 63 of an adder 62 (nxm)) -- it is not -- the time -- a comparator 64 -- with the subtractor 66 which outputs the addition output of an adder 62 as address-data A** based on an output The Amcnt register 67 which makes ****** address-data A** outputted from a subtractor 66 in response to a strobe pulse sc, The selector 68 which chooses one side of address-data A** outputted from a subtractor 66, and ****** of the Amcnt register 67 by the selection pulse sp, It has the adder 70 adding the latch 69 who consists of DF/F which one clock pulse makes carry out period delay of address-data A' outputted from a selector 68, and the address data A0 and the output of a multiplier 58 which were latched, and let the output of an adder 70 be address data A.

[0052] The strobe pulse sa to A offset register 60 is outputted synchronizing with the carry output of F ** counter 55. However, in xcnt=X -1, the number of ** of 1 is carried out, and when it is xcnt!=X -1, the number of ** of ****** Rofset of R offset register 61 is carried out. The enumerated data Fcnt of F ** counter 53 are outputted when, as for the strobe pulse sb to R offset register 61, the enumerated data mcnt of 0 and m ** counter 53 are set to n by the enumerated data Scnt of 0 and S ** counter 52. The enumerated data Scnt of S ** counter 52 are 0, and the strobe pulse sc to the Amcnt register 67 is outputted when the enumerated data mcnt of m ** counter 53 are set to 0. The selection pulse sp to a selector 68 is outputted when it becomes enumerated-data mcnt=m -1 of m ** counter 53, and enumerated-data Scnt!=S -1 of S ** counter 52, and ****** of the Amcnt register 67 is chosen.

[0053] The value and address data A0 by which the number of ** was carried out to A offset register with the adder 62 are added, and an addition result is sent out to a comparator 64 and a subtractor 66. Address data A0 are the address data on the two-dimensional matrix of 203x8, and the addition result of the value (that is, offset to the direction of a slot) and address data A0 which doubled the enumerated data Scnt of S ** counter 54 which counts the number of slots nxm with the multiplier 58 serves as address data A.

[0054] a comparator 64 outputs subtraction directions to a subtractor 66, when the addition output of an adder 62 becomes the above (nxm (= 1624)), and a subtractor 66 is set as a setter 65 from the addition output from an adder 62 in response to subtraction directions -- **** (nxm -1) -- it subtracts. Moreover, when the addition output of an adder 62 is not above (nxm (= 1624)), it does not subtract, but the addition output of an adder 62 is outputted from a subtractor 66 as it is.

[0055] Address-data A** in the generating time of a strobe pulse sc is made the Amcnt register 67 the number of **, and it gets down, and when a selector 68 receives a select signal sp, ****** A** of the Amcnt register 67 is selected and outputted. The output from a selector 68 is made into address-data A'. Address-data A' is latched by latch 69 and uses a latch output as address data A0. Moreover, in response to a strobe pulse sa, as for R offset register 61, the number of ** of the data A0 in the time is carried out. Moreover, ****** of R offset register 61 is outputted to A offset register 60, and the number of ** is carried out to A offset register 60 in response to a strobe pulse sa.

[0056] Although m ** counter 53, S ** counter 54, F ** counter 55, X ** counter 56, and the latch 69 are operating by the common clock pulse, actuation is suspended when day interleave memory writing and a read-out gate pulse are low voltage.

[0057] An operation of the address-data generator 3 is explained based on the flow chart of drawing 9 and drawing 10 .
[0058] If a day interleave is started, ****** Aofset of A offset register 60 will be initialized by 1, and it will be initialized by 0 (step S1)., the enumerated data xcnt x, i.e., the address set number, of X ** counter 56 Moreover, the enumerated data mcnt of m ** counter 53, the enumerated data Scnt of S ** counter 54, and the enumerated data Fcnt of a counter F54 are initialized by 0, latch 69 is also initialized, and address data A0 are also initialized (step S2). Although the number of ** of the data A** at this time is carried out to the Amcnt register 67, the number of ** of 0 will be carried out in this case (step S3). Moreover, since it becomes quantity potential when, as for a strobe pulse sc, the enumerated data Scnt of 0 and S ** counter 52 are set to 0 by the enumerated data mcnt of m ** counter 53, the number of ** to the Amcnt register 67 will be performed for every increment of F ** counter 55.
[0059] ****** to the Amcnt register 67 outputted through the selector 68 is latched by latch 69, and address data A0 decide it (step S4). It is confirmed from a decoder 57 whether to be enumerated-data Fcnt=0 of F ** counter 55, enumerated-data Scnt=0 of S ** counter 54, and enumerated-data mcnt=n=8 of m ** counter 53 (step S5). In step S5, when distinguished from enumerated-data Fcnt=0 of F ** counter 55, enumerated-data Scnt=0 of S ** counter 54, and enumerated-data mcnt=n=8 of m ** counter 53, a strobe pulse sb is outputted, the number of ** of the address data A0 is carried out to R offset register 61 (step S6), and step S7 is performed. However, at this time, since it is enumerated-data mcnt=0 of m ** counter 53, step S7 is performed from step S5.
[0060] Although not illustrated in drawing 9 following step S7, the increment of the enumerated data mcn of m ** counter 53 is carried out, and, subsequently step S8 is performed until the enumerated data mcnt of m ** counter 53 become enumerated-data mcnt=m -1 (= 202) in step S7. ****** by which the number of ** is carried out to address data A0 and A offset register 60 with the adder 62 in step S8 is added (step S8). When addition output A**' of an adder 62 is above (nxm (= 1624)), (nxm -1 (= 1623)) is subtracted from (step S9) and addition output A**', and it performs from step S4 (step S10). When addition output A**' of an adder 62 is not above (nxm (= 1624)), it performs from step S4 following step S9.
[0061] When the actuation so far is tested by comparison to the general formula of said addressing, n of ****** of A offset register 60 is equal to the x-th power (when the x-th power of n exceeds (nxm -1), it is equal to the remainder when repeating and subtracting (nxm -1)), and the x-th power of yxn is equal to the accumulation of the x-th power of n. Moreover, since data A**' does not exceed the twice of (nxm -1), the MODEYURO operation of (nxm -1) can simplify a configuration by subtracting (nxm -1), when (nxm -1) is exceeded. In the last address where data A**' becomes equal to (nxm -1), if (nxm -1) is subtracted, it will be set to 0 and fault will be caused.
[0062] However, that A**' becomes equal to (nxm -1) can avoid this by changing, if (nxm -1) is subtracted from it being only the last address when (nxm) is exceeded for the conditions of subtraction. This is equivalent to having simplified the conditions made into A=y in y=nxm -1 of the general formula of said addressing.
[0063] When the enumerated data mcnt of m ** counter 53 are set to m-1 (= 202), the step of conditional branching based on the enumerated data Scnt of S ** counter 54 is performed (step S11). Step S12 is performed until the enumerated data Scnt of S ** counter 54 are set to S-1 (= 47), and it performs repeatedly following step S12 from step S4. At step S12, the increment of the enumerated data Scnt of S ** counter 54 is carried out, the enumerated data mcnt of m ** counter 53 are reset, and ****** of the Amcnt register 67 is outputted as address-data A' (step S12). That is, ****** of the Amcnt register 67 is chosen by the selector 68. This actuation is for being in a frame and making equal initial value of the address data A of each slot.
[0064] For example, in the 1st frame, the address data A0 of each slot start 0, and it begins from 203 in the 2nd frame. Therefore, in the 2nd frame, whenever a slot replaces, it is necessary to load 203 to address data A0. Since it is enumerated-data Fcnt=0 of F ** counter 55, i.e., the 1st frame, at present, 0 by which the number of ** was carried out to the Amcnt register 67 for every increment of a slot will be loaded. The above-mentioned actuation is repeated until the enumerated data Scnt of S ** counter 54 are

set to S-1 (= 47).
[0065] When the enumerated data Scnt of S ** counter 54 are set to S-1 (= 47), the conditional-branching step based on the enumerated data Fcnt of F ** counter 55 is performed (step S13). When not fulfilling enumerated-data Fcnt=F-1 of F ** counter 55 in step S13, step S14 is performed, the increment of the enumerated data Fcnt of F ** counter 55 is carried out, and reset of the enumerated data Scnt of S ** counter 54 and the enumerated data mcnt of m ** counter 53 is performed (step S14). Then, A offset registerA0 accumulates to 60 (step S15). This is because the initial value of the address data A0 at the time of frame modification turns into the next value of the data A0 of the final value of a front frame.
[0066] That is, when the address set number x is 0, the last address data A0 of the 1st frame are 202, and since ****** of A offset register 60 is 1, the head of two frames is set to 202+1=203. Moreover, as a result of step S15, step S16 is performed, data A'>= (nxm) is checked, as a result of step S16, step S17 is performed alternatively and, subsequently step S3 is performed. What (nxm -1) is subtracted for when data A' exceeds (nxm) (step S17) is the same as that of the aforementioned case. Furthermore, this result serves as a value loaded whenever the number of ** is carried out to the Amcnt register 67 by step S3 and a slot is changed by it.
[0067] When the enumerated data Fcnt of F ** counter 55 become F-1 (= 7) in step S13, at this time, the day interleave for 1 super frame is completed. When the address set number x has not reached x=X -1 (= 179) by conditional branching (step S20) based on the enumerated data xcnt of X ** counter 56, step S21 is performed and the number of ** of the ****** of R offset register 61 by which the number of ** was carried out in step S6 is carried out to A offset register 60 (step S21). Furthermore, the increment of the address set number x is carried out (step S22).
[0068] this actuation -- the general formula of said addressing carried out -- and (one formula) (two formulas) it explains.
[0069] ****** of A offset register 60 is the address data A (value of the x-th power of A=1xn) of the x-th power of n, i.e., the case of y= 1, (although it is equal (like the above)). Are equal to the remainder when repeating subtraction by (nxm -1), when the value of the x-th power of n exceeds (nxm -1). ****** Aofset' of A offset register 60 of the following address set becomes the x-th power of x-th power xn=8x[of ** (x+1) =1xn] n of 1xn similarly, and this is equal to the address data A in y= 8. putting in another way -- if -- current -- y -- = -- eight -- address data -- A -- memorizing -- if -- this -- a degree -- the address -- a set -- a number -- x -- A -- offset -- a register -- 60 -- ****** -- it is -- Aofset -- ' -- becoming -- count -- a circuit -- being omissible -- ******** . Since the address data A at the time of y=mcnt=n=8 were memorized to R offset register 61 by step S5 and step S6, before progressing to the following address set, this is written in A offset register 60. Moreover, all are initialized when the enumerated data xcnt of X ** counter 56 are set to X-1 (= 179).
[0070] Some address data A generated by one gestalt of this operation are shown in drawing 11 and drawing 12 . From the relation of space, the address set number x showed even 17 and the address number y showed even 50.
[0071] According to the day interleave circuit which starts one gestalt of this operation as mentioned above As opposed to the address data A to the day interleave memory 4 which made it generate by the address-data generator 3 A lead (R), The utilization ratio of memory is raised by being carried out by a lead preceding rather than a light, and writing data in the address which became an opening by having read data like a light (W), a lead (R), a light (W), and ....
[0072] On the other hand, two address-data generators are formed, for example, and one is read, and it can carry out only to address-data generating, one can be written in, and it can read to a high speed per super frame as only for address data. In this case, address data must be the same address data. For example, according to the timing shown in drawing 3 , if it reads and writes [both] in and 203 byte processings are carried out, it is a repetition called a 4-byte section pause, but it is also possible to read only read-out continuously, without carrying out 4 bytes of pause.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the configuration of the day interleave circuit concerning one gestalt of operation of this invention.
[Drawing 2] It is the mimetic diagram with which explanation of the I / O data of the buffer memory in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 3] It is the mimetic diagram with which explanation of the timing signal of the timing signal generator in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 4] It is the mimetic diagram with which explanation of the interleave by which a day interleave is carried out in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 5] It is the mimetic diagram with which explanation of the principle of the day interleave in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 6] It is the mimetic diagram with which explanation of the principle of the day interleave in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 7] It is the mimetic diagram of the address space with which explanation of the day interleave in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 8] It is the block diagram showing the configuration of the address-data generator in the day interleave circuit concerning one gestalt of operation of this invention.
[Drawing 9] It is the flow chart with which explanation of the address-data generating operation in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 10] It is the flow chart with which explanation of the address-data generating operation in the day interleave circuit concerning one gestalt of operation of this invention is presented.
[Drawing 11] It is the mimetic diagram showing a part of generating address in the day interleave circuit concerning one gestalt of operation of this invention.
[Drawing 12] It is the mimetic diagram showing a part of generating address in the day interleave circuit concerning one gestalt of operation of this invention.
[Description of Notations]
1 Timing Signal Generator
2 Buffer Memory
3 Address-Data Generator
4 Memory for Day Interleave
50 Strobe Pulse Generating Section
51 Slot Number Detecting Element
52 MODEYURO Operation Part
53 54 m ** counter, S ** counter
55 56 F ** counter, X ** counter
57 Decoder
58 Multiplier

59, 63, 65 Setter
60 61 A offset register, R offset register
62 70 Adder
64 Comparator
66 Subtractor
67 Amcnt Register
68 Selector
69 Latch

[Translation done.]

* NOTICES *

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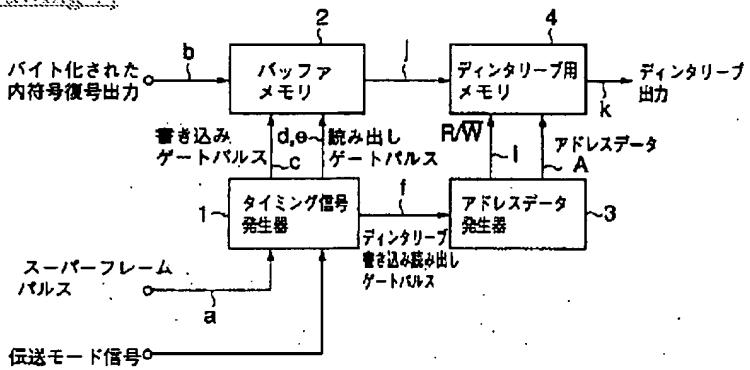
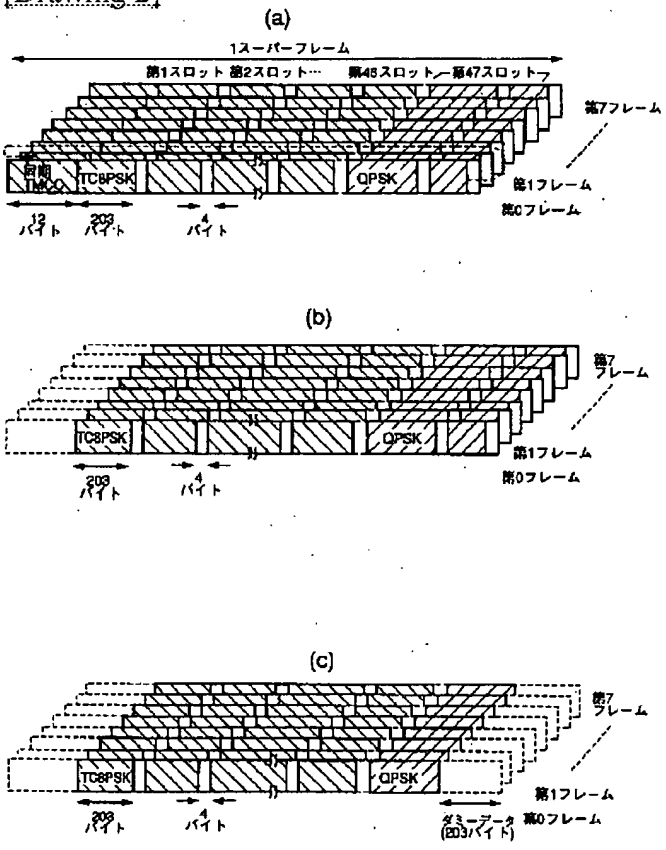
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]

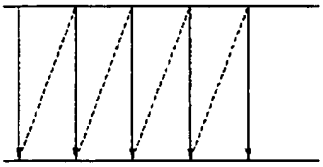


[Drawing 4]

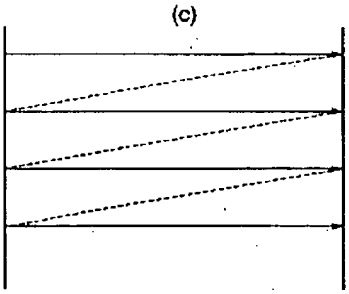
(a)

A[0] D[0]	*A[1]* D[1]	*A[2]* D[2]	*A[3]* D[3]	*A[4]* D[4]
A[5] D[5]	*A[6]* D[6]	*A[7]* D[7]	*A[8]* D[8]	*A[9]* D[9]
A[10] D[10]	*A[11]* D[11]	*A[12]* D[12]	*A[13]* D[13]	*A[14]* D[14]
A[15] D[15]	*A[16]* D[16]	*A[17]* D[17]	*A[18]* D[18]	*A[19]* D[19]

(b)



(c)



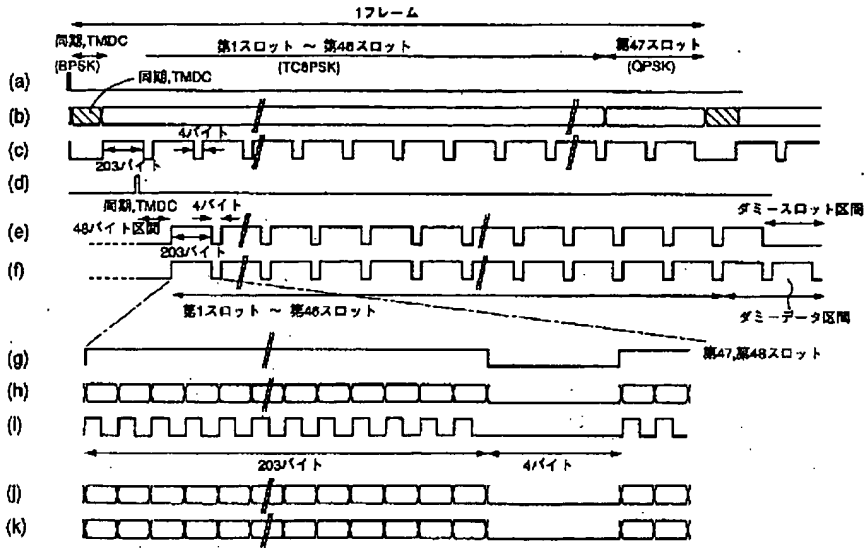
[Drawing 6]

アドレスセット番号x

アドレス番号y

	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	0	0	0	0
1	1	4	16	7	9	17	11	6	5	1
2	2	8	13	14	18	15	3	12	10	2
3	3	12	10	2	8	13	14	18	15	3
4	4	16	7	9	17	11	6	5	1	4
5	5	1	4	16	7	9	17	11	6	5
6	6	5	1	4	16	7	9	17	11	8
7	7	9	17	11	6	5	1	4	16	7
8	8	13	14	18	15	3	12	10	2	8
9	9	17	11	6	5	1	4	16	7	9
10	10	2	8	13	14	18	15	3	12	10
11	11	6	5	1	4	16	7	9	17	11
12	12	10	2	8	13	14	18	15	3	12
13	13	14	18	15	3	12	10	2	8	13
14	14	18	15	3	12	10	2	8	13	14
15	15	3	12	10	2	8	13	14	18	15
16	16	7	9	17	11	6	5	1	4	16
17	17	11	6	5	1	4	16	7	9	17
18	18	15	3	12	10	2	8	13	14	18
19	19	19	19	19	19	19	19	19	19	19

[Drawing 3]



[Drawing 5]

(a)

m=5（書き込み方向）

A[0] D[0]	A[1] D[5]	A[2] D[10]	A[3] D[15]	A[4] D[1]
A[5] D[6]	A[6] D[11]	A[7] D[16]	A[8] D[2]	A[9] D[7]
A[10] D[12]	A[11] D[17]	A[12] D[3]	A[13] D[8]	A[14] D[13]
A[15] D[18]	A[16] D[4]	A[17] D[9]	A[18] D[14]	A[19] D[19]

読み出し n=4

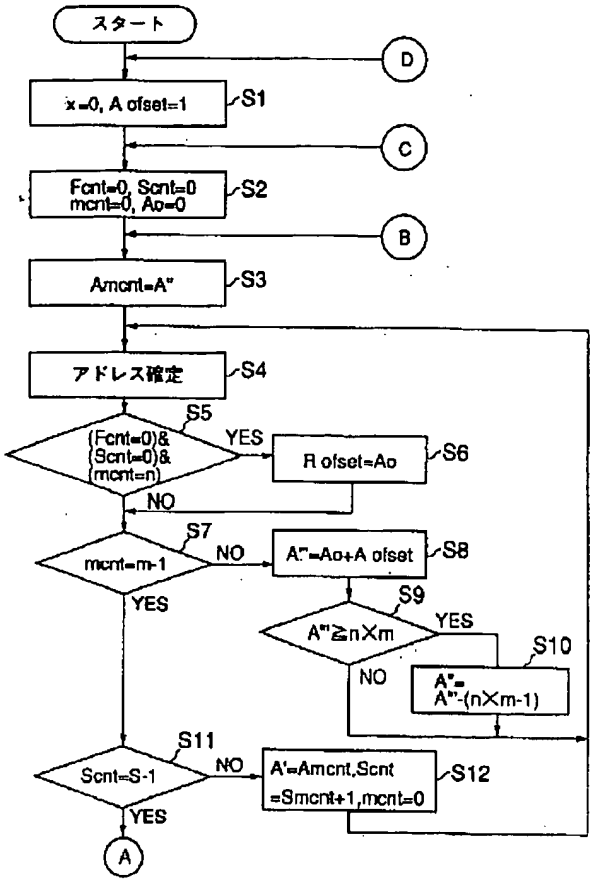
(b)

A[0] D'[0]	A[1] D'[6]	A[2] D'[12]	A[3] D'[18]	A[4] D'[5]
A[5] D'[11]	A[6] D'[17]	A[7] D'[4]	A[8] D'[10]	A[9] D'[16]
A[10] D'[3]	A[11] D'[9]	A[12] D'[15]	A[13] D'[2]	A[14] D'[8]
A[15] D'[14]	A[16] D'[1]	A[17] D'[7]	A[18] D'[13]	A[19] D'[19]

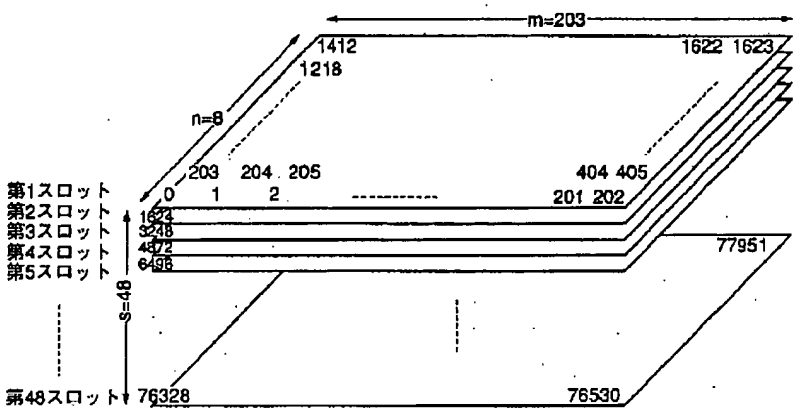
(c)

A[0] D"[0]	A[1] D"[11]	A[2] D"[3]	A[3] D"[14]	A[4] D"[6]
A[5] D"[17]	A[6] D"[9]	A[7] D"[1]	A[8] D"[12]	A[9] D"[4]
A[10] D[15]	A[11] D[7]	A[12] D[16]	A[13] D[10]	A[14] D[2]
A[15] D"[13]	A[16] D"[5]	A[17] D"[16]	A[18] D"[8]	A[19] D"[19]

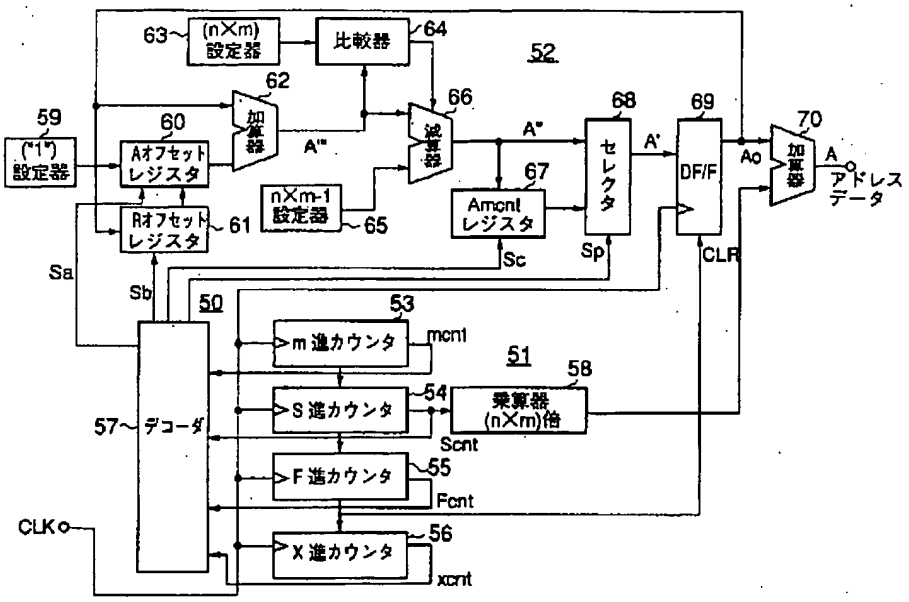
[Drawing 9]



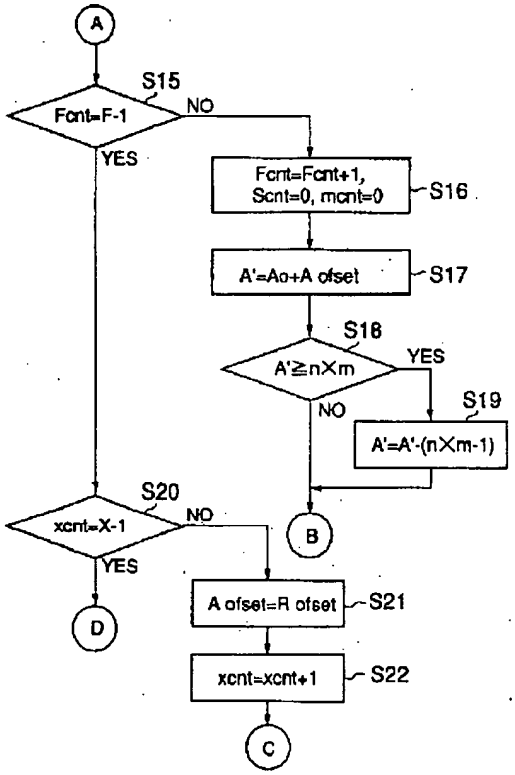
[Drawing 7]



[Drawing 8]



[Drawing 10]



[Drawing 11]

アドレスセット番号x

アドレス番号y	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	8	64	512	850	308	841	236	265	497	730	971	1276	470	514	868	436	242
2	2	16	128	1024	77	616	59	472	530	994	1460	319	929	940	1028	109	872	484
3	3	24	192	1536	927	924	900	708	795	1491	567	1290	582	1410	1542	975	1308	726
4	4	32	256	425	154	1232	118	944	1060	365	1297	638	235	257	433	218	121	968
5	5	40	320	937	1004	1540	959	1180	1325	862	404	1609	1511	727	947	1084	557	1210
6	6	48	384	1449	231	225	177	1416	1590	1359	1134	957	1164	197	1461	327	993	1452
7	7	56	448	338	1081	533	1018	29	232	233	241	305	817	44	352	1193	1429	71
8	8	64	512	850	308	841	236	265	497	730	971	1276	470	514	868	436	242	313
9	9	72	576	1362	1156	1149	1077	501	762	1227	78	624	123	984	1380	1302	678	555
10	10	80	640	251	385	1457	295	737	1027	101	808	1595	1399	1454	271	545	1114	797
11	11	88	704	763	1235	142	1138	973	1292	598	1538	943	1052	301	785	1411	1550	1039
12	12	96	768	1275	462	450	354	1209	1557	1095	645	291	705	771	1299	654	363	1281
13	13	104	832	164	1312	758	1195	1445	199	1592	1375	1262	358	1241	190	1520	799	1523
14	14	112	896	676	539	1068	413	58	464	466	482	610	11	88	704	763	1235	142
15	15	120	960	1188	1389	1374	1254	294	729	963	1212	1581	1287	558	1218	6	48	384
16	16	128	1024	77	616	59	472	530	994	1460	319	929	940	1028	109	872	484	626
17	17	136	1088	589	1466	367	1313	766	1259	334	1049	277	593	1498	623	115	920	868
18	18	144	1152	101	693	675	531	1002	1524	831	158	248	246	345	1137	981	1356	1110
19	19	152	1216	1613	1543	983	1372	1238	166	1328	886	596	1522	815	28	224	169	1352
20	20	160	1280	502	770	1291	590	1474	431	202	1616	1567	1175	1285	542	1090	605	1594
21	21	168	1344	1014	1620	1599	1431	87	696	698	723	915	828	132	1056	333	1041	213
22	22	176	1408	1526	847	284	649	323	961	1196	1453	263	481	602	1570	1199	1477	455
23	23	184	1472	415	74	592	1490	559	1226	70	560	1234	134	1072	461	442	290	697

[Drawing 12]

アドレスセット番号x

アドレス番号y	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
24	24	192	1536	927	924	900	708	795	1491	567	1290	582	1410	1542	975	1308	726	939									
25	25	200	1600	1439	151	1208	1549	1031	133	1064	397	1553	1063	389	1489	551	1162	1181									
26	26	208	41	328	1001	1516	767	1267	398	1561	1127	901	716	859	380	1417	1598	1423									
27	27	216	105	840	228	201	1608	1503	663	435	234	249	369	1329	894	660	411	42									
28	28	224	169	1352	1078	509	826	116	928	932	964	1220	22	176	1408	1526	847	284									
29	29	232	233	241	305	817	44	352	1193	1429	71	568	1298	646	299	769	1283	526									
30	30	240	297	753	1155	1125	885	586	1458	303	801	1539	951	1116	813	12	96	768									
31	31	248	361	1265	382	1433	103	824	100	800	1531	887	604	1586	1327	877	532	1010									
32	32	256	425	154	1232	118	944	1060	385	1297	638	235	257	433	218	121	968	1252									
33	33	264	489	666	459	426	162	1296	630	171	1368	1206	1533	903	732	987	1404	1494									
34	34	272	553	1178	1309	734	1003	1532	895	668	475	554	1186	1373	1246	230	217	113									
35	35	280	617	67	536	1042	221	145	1160	1165	1205	1525	839	220	137	1096	653	355									
36	36	288	681	579	1386	1350	1062	381	1425	39	312	873	492	690	651	339	1089	597									
37	37	296	745	1091	613	35	280	617	67	536	1042	221	145	1160	1165	1205	1525	839									
38	38	304	809	1603	1463	343	1121	853	332	1033	149	1192	1421	7	56	448	338	1081									
39	39	312	873	492	690	651	339	1089	597	1530	879	540	1074	477	570	1314	774	1323									
40	40	320	937	1004	1540	959	1180	1325	862	404	1609	1511	727	947	1084	557	1210	1565									
41	41	328	1001	1516	767	1267	398	1561	1127	901	716	859	380	1417	1598	1423	23	184									
42	42	336	1065	405	1617	1575	1239	174	1392	1398	1446	207	33	264	489	668	459	426									
43	43	344	1129	917	844	260	457	410	34	272	553	1178	1309	734	1003	1532	895	668									
44	44	352	1193	1429	71	568	1298	646	299	769	1283	526	962	1204	1517	775	1331	910									
45	45	360	1257	318	921	676	516	882	564	1266	390	1497	615	51	408	18	144	1152									
46	46	368	1321	830	148	1184	1357	1118	829	140	1120	845	268	521	922	884	580	1394									
47	47	376	1385	1342	998	1492	575	1354	1094	637	227	193	1544	991	1436	127	1016	13									
48	48	384	1449	231	225	177	1418	1590	1359	1134	957	1164	1197	1461	327	993	1452	255									
49	49	392	1513	743	1075	485	634	203	1	8	64	512	850	308	841	236	265	497									
50	50	400	1577	1255	302	793	1475	439	266	505	794	1483	503	778	1355	1102	701	739									

[Translation done.]